

Final Demo

The Professor will sit down with each group to look over your final verilog simulation runs, chip layout and full-custom blocks. You should be ready to discuss everything that is required for this CAD assignment and any other project-related issues. You don't need to do any special preparation for this (i.e. don't review old CAD assignments, etc.) but plan to spend an hour or so in the lab. Try to have relevant simulations, schematics and layouts up and ready to look at. If there are problems or there are things you were unable to finish, you should tell the Professor about those. It is better for you to tell the Professor about those than for the Professor to find them on their own when they review your design in more depth outside of the demo. This is also a good time for you to highlight any aspects of your design that you think went particularly well or those that didn't go so well and how you might have done things differently.